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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/775,496	02/05/2001	Eugene Zilberman	246/85	8466

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EXAMINER	
LOHN, JOSHUA A	
ART UNIT	**PAPER NUMBER**
2184	3

DATE MAILED: 11/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/775,496	Applicant(s) ZILBERMAN, EUGENE	
	Examiner Joshua A Lohn	Art Unit 2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4, and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Ajanovic, United States Patent number 6,298,426, filed December 31, 1997.

As per claim 1, Ajanovic discloses at least one main board that includes a processing system for enabling interaction with the host system, see Memory Controller (104) of figure 2. Ajanovic also discloses at least one memory board separate from the main board, with the memory board containing at least part of the storage systems primary solid-state component array used for data storage, see Memory Modules (200 A-D) of figure 2, which are independent boards that make up the solid-state memory for data storage, see column 4, lines 51-61. Ajanovic also discloses for each memory board having at least one secondary non-volatile memory device, located on the memory board, containing system information related to each memory board, see column 3, lines 61-66, where the NVRAM contains system information.

As per claim 2, Ajanovic discloses a memory board including at least a portion of the primary solid-state components array, see column 4, lines 61-61, where the for memory boards, or modules, make up the primary solid-state memory. Ajanovic also discloses at least one respective secondary non-volatile memory device containing system information related to the

main board, see column 3, lines 63-66, which describe the system information stored on the secondary non-volatile memory.

As per claim 4, Ajanovic discloses placing a secondary non-volatile memory device onto each board of the multi-board solid state storage system, see elements 201 A-D of figure 2. Ajanovic discloses recording system information of each board on the secondary non-volatile memory device, see column 3, lines 64-66. Ajanovic discloses storing this system information in the secondary non-volatile memory device, see column 3, lines 61-66.

As per claim 5, Ajanovic discloses that the memory modules can take on multiple, different organizations, see column 3, lines 33-42. This would inherently include the ability to add, connect, and replace boards to provide for the different organizations. Ajanovic also discloses testing the boards by providing error detection on the data retrieved from the memory boards, see column 5, lines 18-21.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ajanovic in view of Jeddeloh, United States Patent number 6,052,798, filed July 1, 1998, in further view of Okaue et al., United States Patent number 6,601,140, filed April 6, 2000.

As per claim 3, Ajanovic discloses the secondary non-volatile memory device storing information including a description of the geometry of the primary solid-state components array,

see column 3, line 65, where the memory data width and memory size help define the geometry. Ajanovic also discloses storing manufacturing information for the board, such as the type of memory module being used, see column 3, lines 64-65. Ajanovic fails to disclose the non-volatile memory containing security information for the data stored on the board and containing fault location record for the primary solid-state components array located on the board.

Jeddeloh discloses using a secondary non-volatile memory to store a fault location record for the primary solid-state components array located on the board, see element 18 of figure 1 and column 3, lines 1-3.

It would have been obvious at the time the invention was made to include the fault location record of Jeddeloh in the memory module of Ajanovic.

This would have been obvious because Ajanovic discloses a memory module that contains a non-volatile memory for storing system information, as mentioned above. Jeddeloh discloses that including a fault map in a non-volatile secondary memory of a memory module allows for eliminating the need for redundant rows and extra bits for error correction schemes, see column 1, line 40 through column 2, line 4. It would be obvious to implement the fault map in the non-volatile memory of Ajanovic to eliminate this high memory overhead and still allow for detection and avoidance of faulty memory cells. Ajanovic and Jeddeloh fail to disclose using the secondary non-volatile memory to include security information.

Okaue discloses using a secondary non-volatile memory that includes security information for data stored on the memory board, in the form of security keys, see column 7, lines 7-10.

It would have been obvious at the time the invention was made to include the security information of Okaue with the memory module of Ajanovic and Jeddeloh.

This would have been obvious because it is well known that a desire exists to have memory modules that are secure for general use, see column 1, lines 25-36. A secure memory card would require security information to be contained within. It would have been obvious to include the security information, which is stored in a non-volatile memory block of the memory card of Okaue, in the memory card of Ajanovic and Jeddeloh to provide for a memory card that is capable of producing any desired levels of security.

As per claim 6, the combined invention of Ajanovic, Jeddeloh, and Okaue provides system information that includes fault locations, geometry information, manufacturing information, and security information, as described in the rejection of claim 3 above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure is listed on form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua A Lohn whose telephone number is (703) 305-3188. The examiner can normally be reached on M-F 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoleil can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

JAL

SCOTT BADERMAN
PRIMARY EXAMINER